Reg. No: ⬚⬚⬚⬚⬚⬚⬚⬚⬚⬚

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
BTECH II Year I Semester Supplementary Examinations June 2019
SWITCHING THEORY AND LOGIC DESIGN
(Electronics & Communication Engineering)

Time: 3 hours   Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1 **a** Perform the following using BCD arithmetic   6M
     (i) $(79)_{10} + (177)_{10}$ (ii) $(481)_{10} + (178)_{10}$

    b Subtraction by using 2's complement for the given   6M
     i)111001-1010   ii) 10011-10001   iii)1001-101000

OR

2 **a** State Duality theorem. List Boolean laws and their Duals.   6M
    b Give the truth table of logic gates.   6M

UNIT-II

3 Minimize the given Boolean function F (A, B,C,D) = Σ m(0,1,2,3,6,7,13,15) using   12M
tabulation method and implement using basic gates.

OR

4 Simplify the following Boolean function for minimal SOP& POS form using K-map
    i)   F (A, B, C, D) = Σ (0,1,2,4,5,6,8,9,12,13,14)   12M
    ii) F (A, B, C, D) = π(1,3,6,9,11,12,14)

UNIT-III

5 **a** Design & implement BCD to Excess-3 code converter.   6M
    b Design & implement 4-bit Binary Adder-subtractor.   6M

OR

6 **a** What is Decoder? Design three to eight-line Decoder.   6M
    b Design & implement BCD To seven segment decoder.   6M

UNIT-IV

7 **a** a) Draw the logic symbol, characteristics table and derive characteristics equation of JK   6M
flip flop.   .

    b b) Design T Flip Flop by using JK Flip Flop and draw the timing diagram.   6M

OR

8 **a** Implement 6-bit ring counter using suitable shift register. Briefly describe its operation.   10M
    b Write the difference between Latch and Flip flop   2M

UNIT-V

9 Implement the following Boolean function using PLA   12M
(i)F1= Σm(0,1,2,3,8,10,12,14)   (ii)F2 = Σm(0,1,2,3,4,6,8,10,12,14).

OR

10 Give the logic implementation of a 32x4 bit ROM using a decoder with necessary diagram.   12M

*** END ***